MTM5P18
MTM5P20
MTP5P18
MTP5P20

Designer's Data Sheet

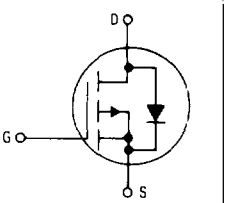
Power Field Effect Transistor
P-Channel Enhancement-Mode Silicon Gate TMOS

TMOS™

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 1 OHM
180 and 200 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

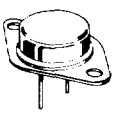


MAXIMUM RATINGS

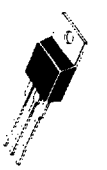
Rating	Symbol	MTM or MTP 5P18	MTM or MTP 5P20	Unit
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	180	200	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current — Continuous	I_D	5		Adc
Pulsed	I_{DM}	20		
Total Power Dissipation @ T_C = 25°C	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T_L	275	°C



MTM5P18
MTM5P20
CASE 1-04
TO-204AA



MTP5P18
MTP5P20
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP5P18	$V_{(BR)DSS}$	180	—	Vdc
MTM/MTP5P20		200	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$r_{DS(on)}$	—	1	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 5 Adc)		—	5	
(I_D = 2.5 Adc, T_J = 100°C)		—	4	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1000	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{oss}	—	250	
Reverse Transfer Capacitance	C_{rss}	—	75	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	—	40	ns
Rise Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 11 and 12	t_r	—	50	
Turn-Off Delay Time	$t_{d(off)}$	—	90	
Fall Time	t_f	—	60	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D V_{GS} = 0)	V_{SD}	2 (Typ)	4	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	(Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25" from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

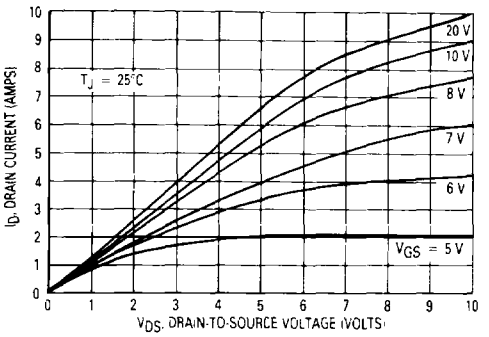


Figure 1. On-Region Characteristics

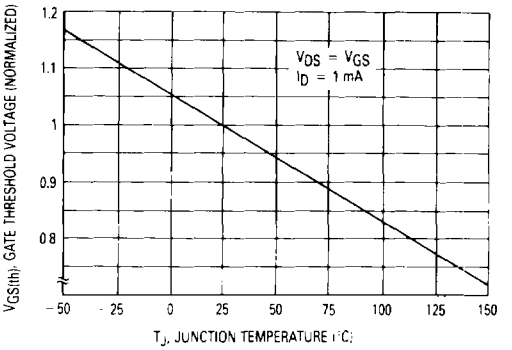


Figure 2. Gate-Threshold Voltage Variation With Temperature

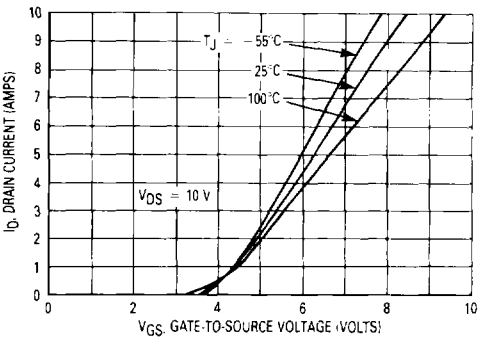


Figure 3. Transfer Characteristics

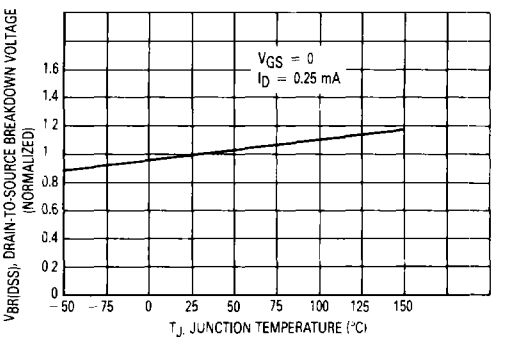


Figure 4. Normalized Breakdown Voltage versus Temperature

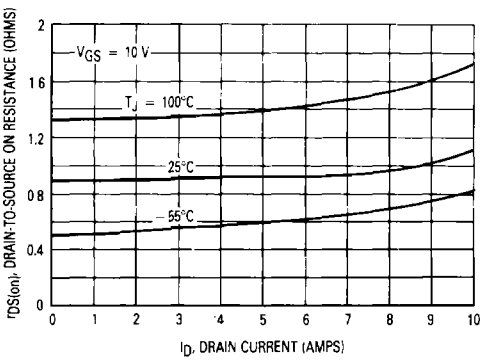


Figure 5. On-Resistance versus Drain Current

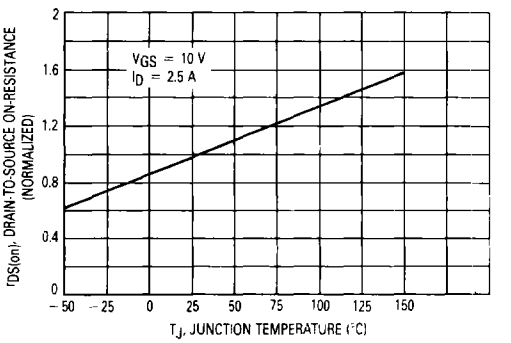


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

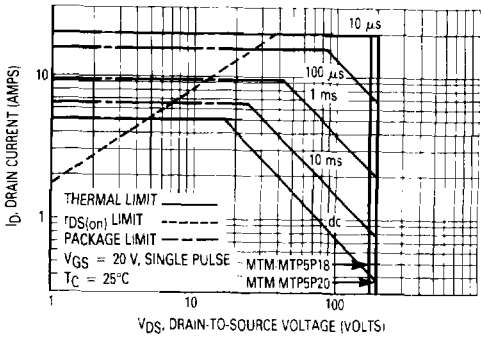


Figure 7. Maximum Rated Forward Biased Safe Operating Area

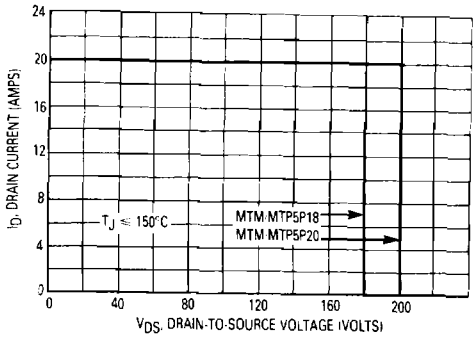


Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 6.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 9.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 7 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

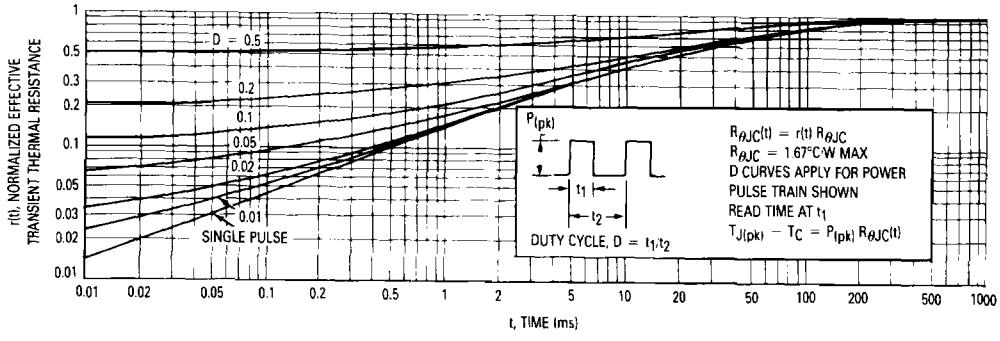

Figure 9. Thermal Response

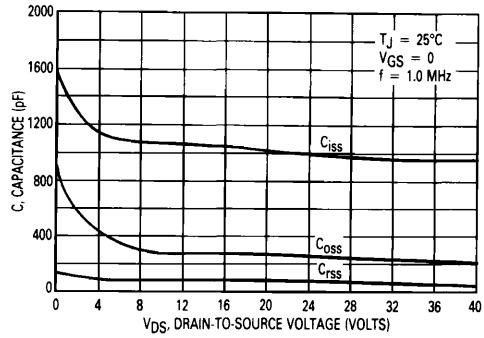

Figure 10. Capacitance Variation

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RESISTIVE SWITCHING

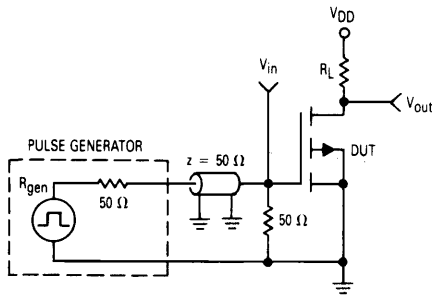


Figure 11. Switching Test Circuit

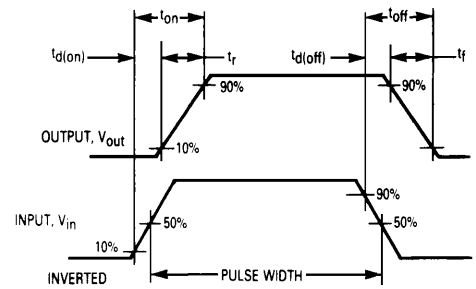
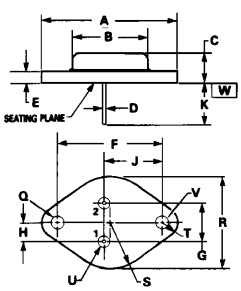


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS

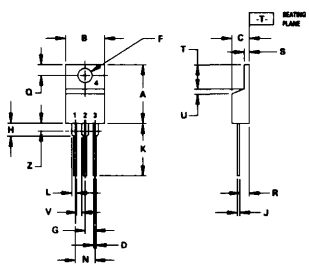


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | ⌀ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ⌀ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓥ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB